In Fall 2024, I took my last class at Iowa State University as apart of my Computer Engineering graduate degree. The course was focused on hardware applications of machine learning systems, and throughout 6 different labs a partner and myself integrated a image inference convolutional neural network in python, C++, and in Verilog utilizing a Xilinx FPGA and Digilent ZedBoard. As part of our final project, we created a multiply accumulate module that was synthesized and constrained with the same open-source digital ASIC design process I utilized for senior design and graduate resource. This enabled us to create a design for a future ASIC tapeout that my partner can verify in person in the Spring 2025 semester. As part of the design process, we defined our design, created an automated suite of tests, and helped integrate the design into the final tapeout submission. The included image on this page is the GDSII layout of our design cell in the open source SkyWater 130nm process.